How to Connect PL to PS using Zynq 7020

# Creating Vivado Project:

Select Device as following

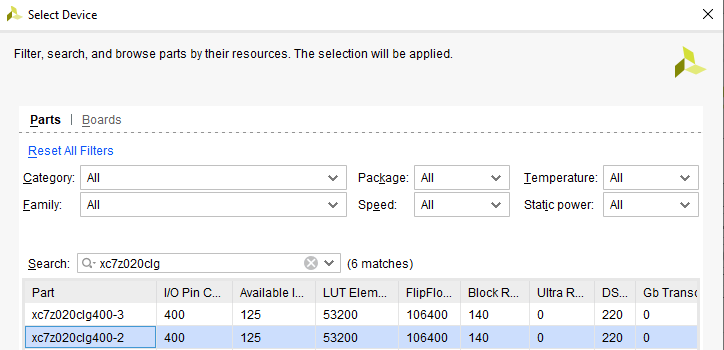


Figure : Selecting Target Device

# Create Block Design:

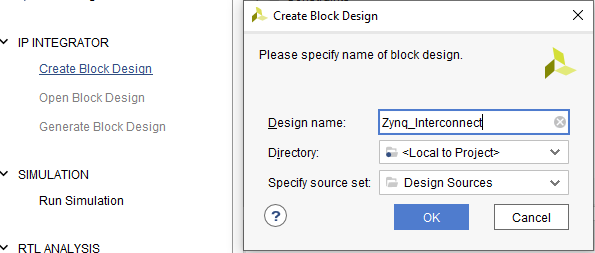


Figure : Creating Block Design for the Project

Click OK and continue.

Once you are in Block Design. It should look like this.

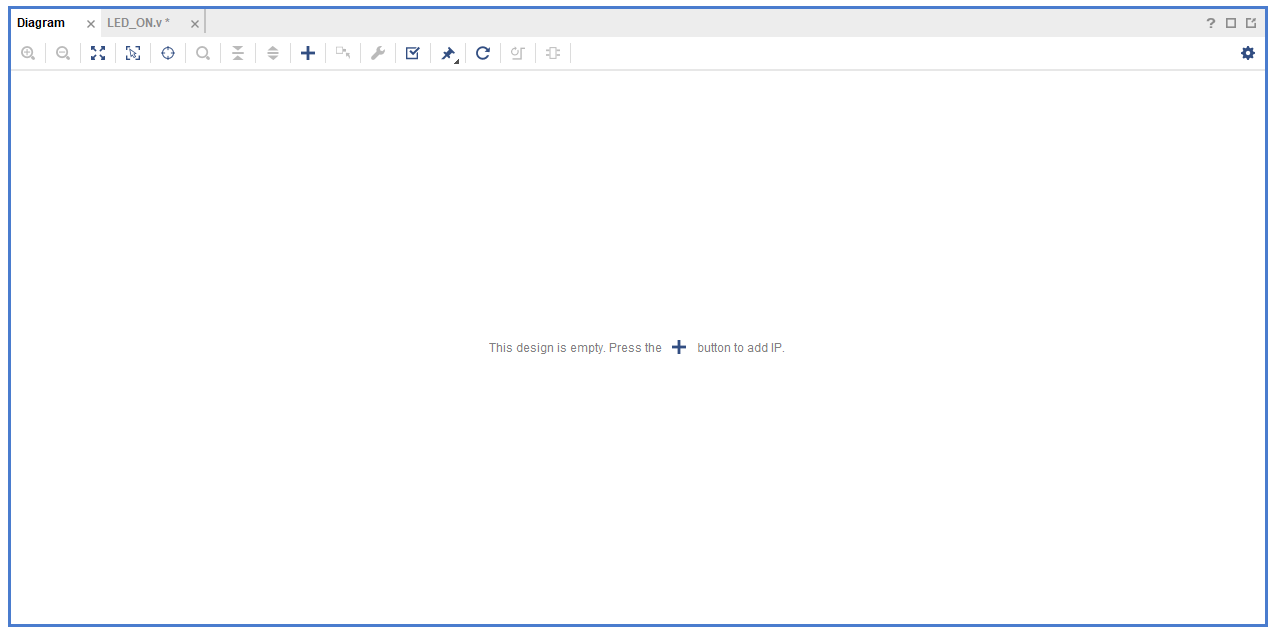


Figure : Default Block Design Screen

Adding IP

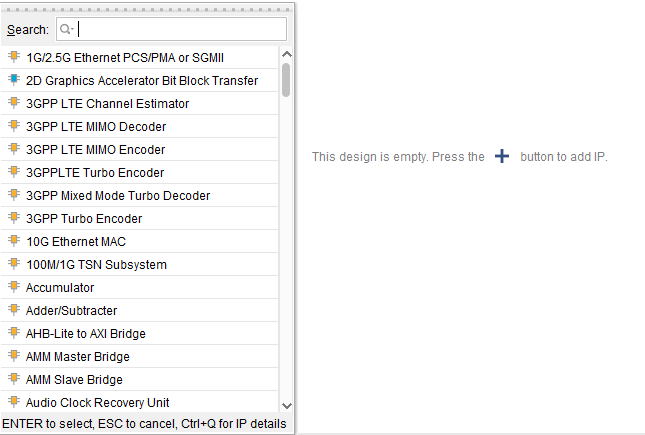


Figure : Adding IP to the block Design

Search and add the following Ips:

* ZYNQ7 Processing System
* AXI GPIO x2
* Utility vector Logic

It should look like this

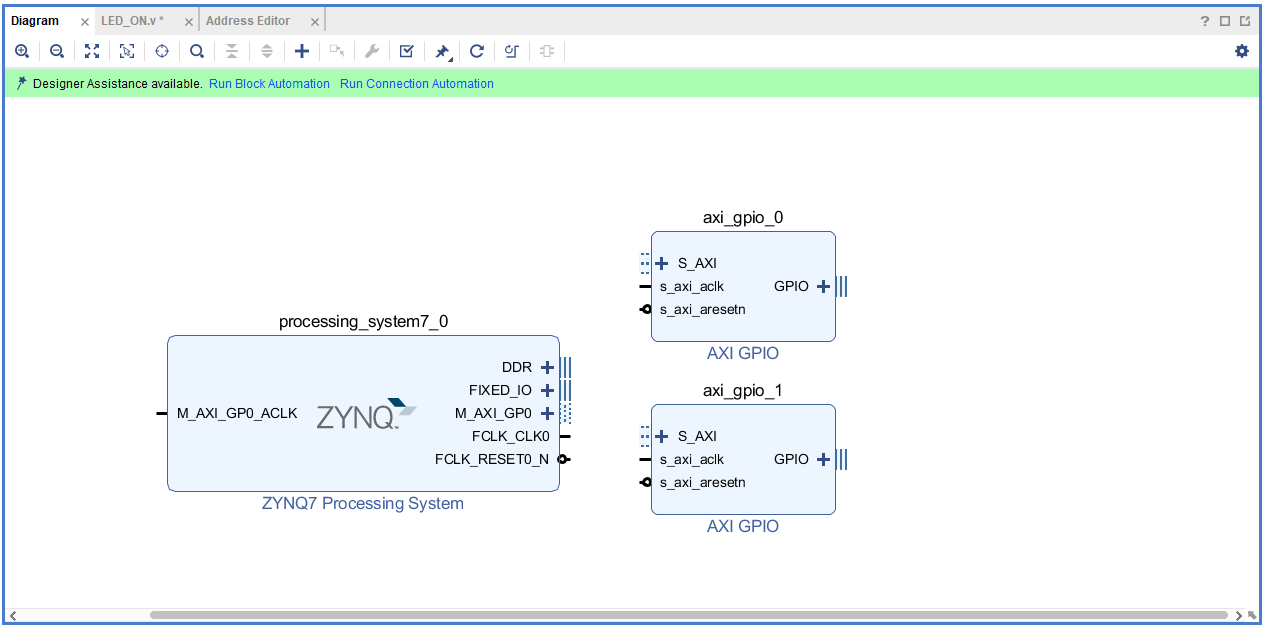


Figure : Zynq PS and AXI GPIO IP in block Design

Now, the designer assistance available option should be good. But we need to configure DDR First.

Enable this in PS IP.

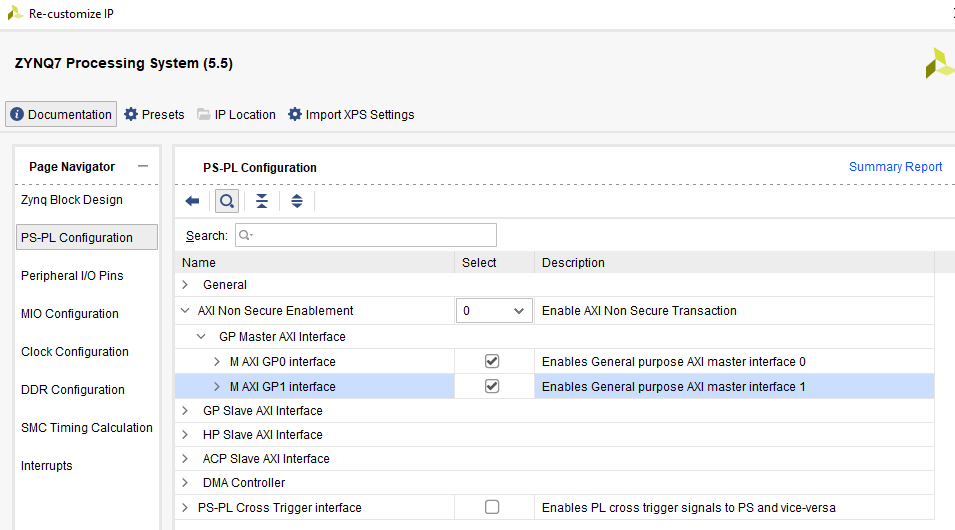


Figure : Enable AXI GPIO in PS

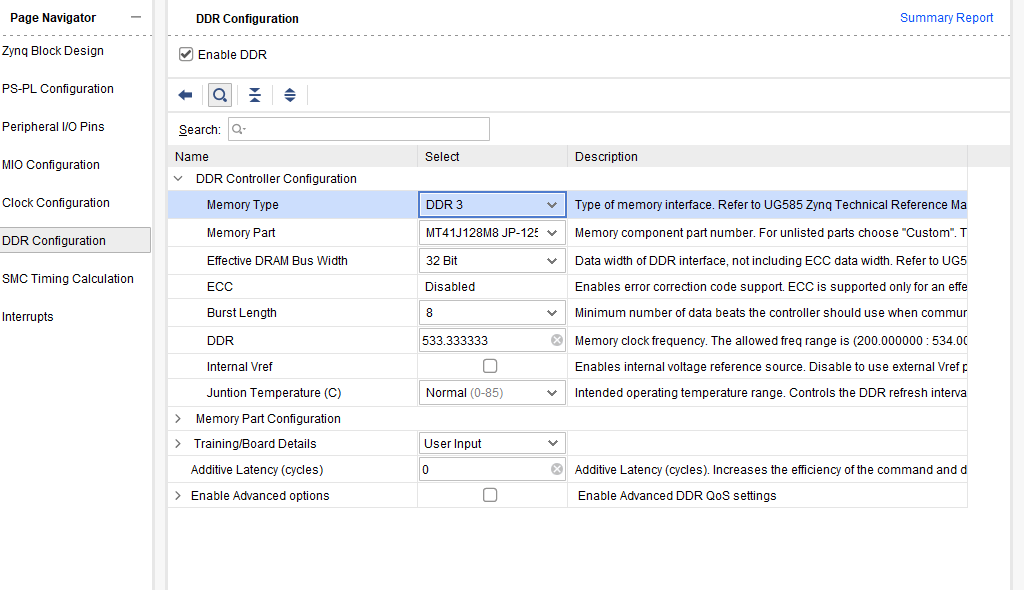


Figure : Configuring DDR in PS

Now, we need to run block automation and select the following options

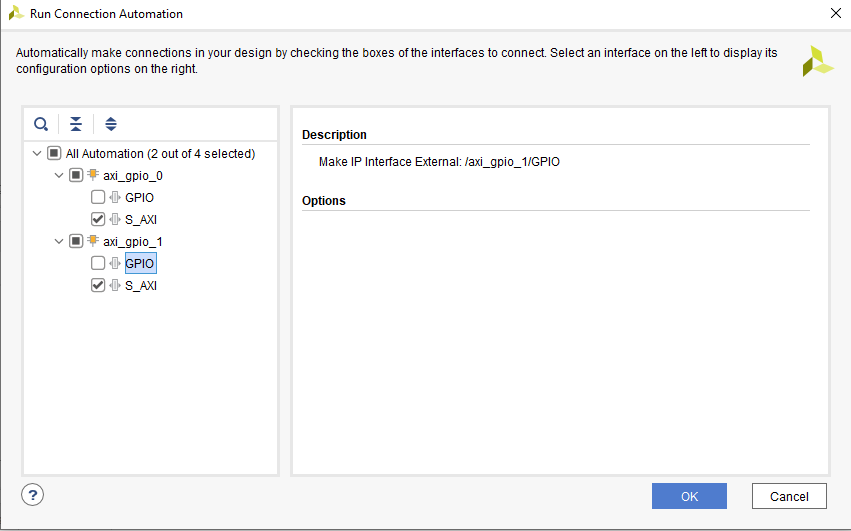


Figure : Selecting Run connection Automation Connections in Block Design

After selecting these options, the diagram should be as follows:

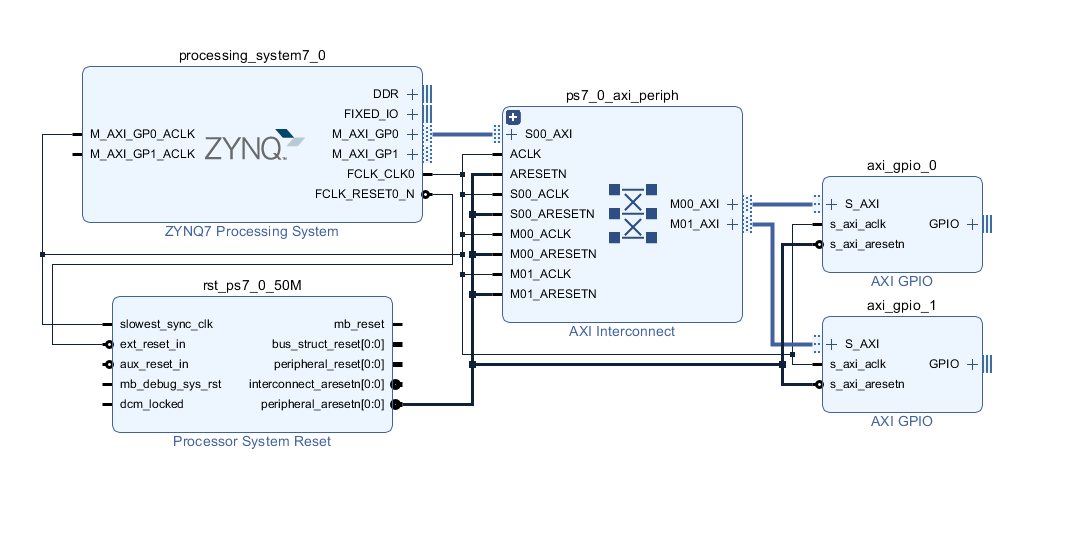


Figure : PS GPIO Configuration

Add utility vector logic Ip and set it as not gate you should have something like this.

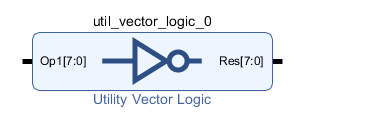


Figure : Utility Vector Logic IP

Connect its input to switch and output to AXI GPIO.

Use the second GPIO to connect it to LED.

Select GPIO 0 as following settings.

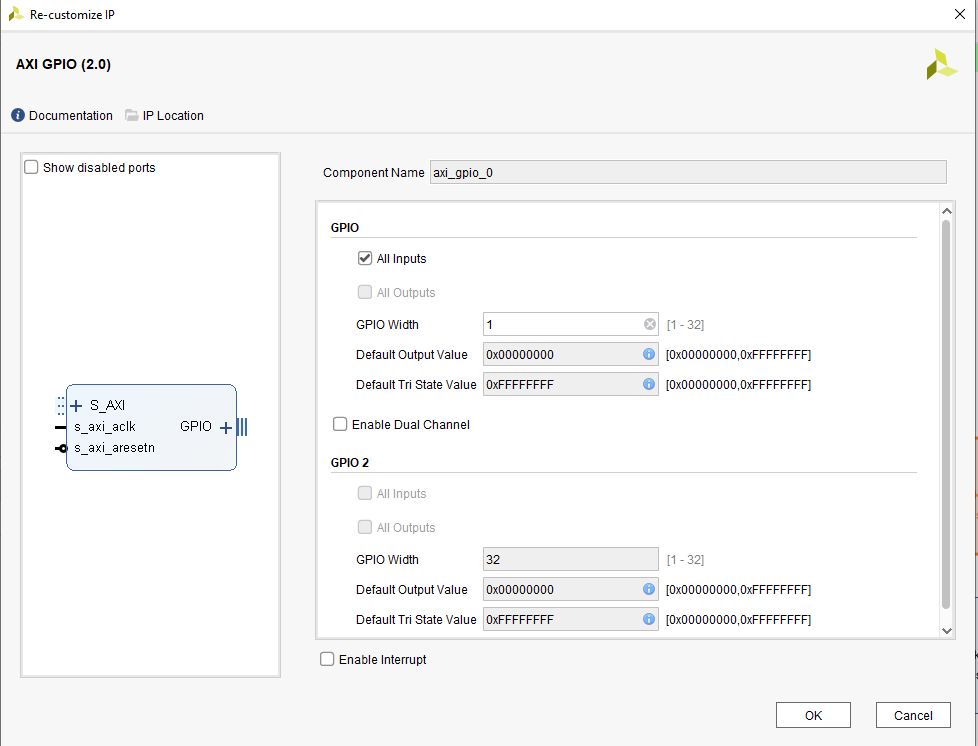


Figure : GPIO 0 settings as an Input to PS

And GPIO 1 as following settings:

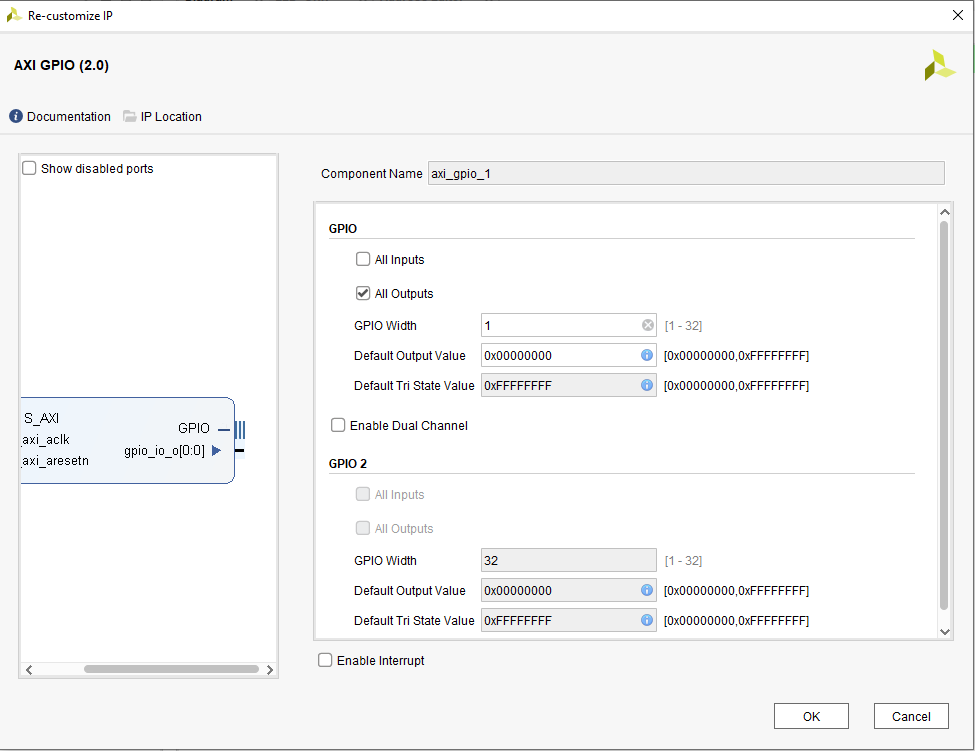


Figure : GPIO 1 configuration as on output

All in together the block design should come out to this.

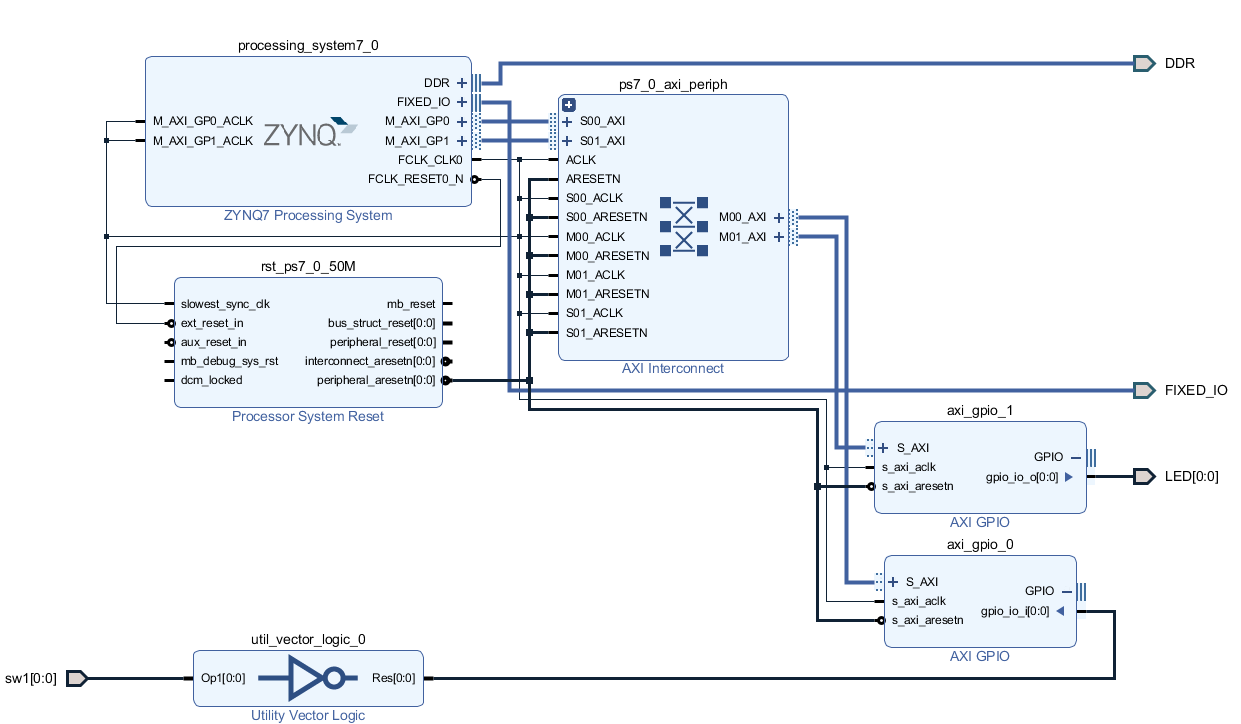


Figure : Completed Design

Now, write its constraint file and it should be ready for bitstream.